# Overview of Radiation Tolerant Unlimited Write Cycle Non-Volatile Memory[§]

Karl F. Strauss, (818) 354-4973 & Taher Daud, (818) 354-5782

karl.strauss@jpl.nasa.gov & taher.daud@jpl.nasa.gov

Jet Propulsion Laboratory, California Institute of Technology

4800 Oak Grove Drive, Pasadena, California 91109

## ABSTRACT

A new concept in avionics development, X2000, is described. Further, a need for non-volatile radiation hardened memory is brought forth. A 1 Mega-bit/in$^2$ memory density specification: 10 year lifetime, 1-MegaRad total ionizing radiation dose survivability, and > $10^{13}$ cycles is drawn for such NASA's missions as Europa Orbiter as the first delivery for X2000. Development effort by JPL for three new technologies for such memory requirement is described.

## INTRODUCTION

As the thirst for knowledge drives NASA into the further reaches of deep space; as the ability and demands for a spacecraft to think smarter increases; as the demands for machine intervention over human correction increase; as the need to precisely log events increases; as the demands for time on the Deep Space Network increase; as missions thrust spacecraft into increasingly hostile environments; as the length of the mission increases in years; as the sophistication of on-board fault protection and recovery increases, so must the ability of on-board spacecraft management system increase.

NASA has completed an initial reconnaissance of our solar system during its 30-year space exploration phase. In the next phase, missions with more detailed scientific quests will be launched. These missions will be required to perform many more challenging tasks such as landing on a celestial body, collecting material samples and returning it to Earth, or exploring objects that have hostile environments [1].

To carry out such technically difficult missions at an affordable cost, NASA has created the Deep Space Systems Technology (DSST) Program, informally known as X2000. Every two to three years, starting in the year 2000, the program will develop and deliver advanced spacecraft avionic systems bound for different missions to explore the solar system and beyond.

In the past, spacecraft systems were unique to the mission they were built for. By contrast, the advanced hardware and software that X2000 will develop, will be adaptable for the varied purposes of several different missions. In sharing common systems and equipment, these ambitious missions will manage to reduce costs.

## NEED FOR NON-VOLATILE MEMORIES

For NASA's long-life and deep-space missions, the ability to store state, sequence, and machine status information on-board the spacecraft for the purposes of project planning and fault recovery pose new challenges on memory technology.

New requirements on spacecraft memory systems are emerging every day – some that seemed unfathomable just a few years ago. The need to precisely know where a spacecraft is in its trajectory, or the need to know what sequence was in operation during a spacecraft fault, is increasingly becoming the rule and not the exception.

Most current fault-intervention schemes require the spacecraft to enter a "Safe Mode" and send a signal to a listening station on Earth, requesting help. Here, mission planners detect the problem and issue instructions allowing the spacecraft to work around the error; all the while, perhaps invaluable science data – perhaps the main reason for the mission itself – could be lost.

Using average planetary distances, the time for a signal from a spacecraft to reach Earth is under 12 minutes for the inner planets, 43 minutes from Jupiter, and an incredible 4 hours from Pluto. In theory it would be possible for a Mars-orbiting spacecraft to request help, have a response calculated, and received by the spacecraft all within a half-

[§] 0-7803-5846-5/00/$10.00 © 2000 IEEE

hour period. However, man's curiosity is not limited to our nearest neighbors. The Pluto Kuiper Express mission being planned by the Jet Propulsion Laboratory will have a rendezvous with Pluto, the last planet not yet visited by Man, early in this Century. No previous mission has had the visitation of this planet as its goal. Should a spacecraft fault occur, with a round-trip light time of over eight hours, significant amounts of science data can be lost before a response to a call for help is received – the mission could be lost.

It was with the goal of maximizing the spacecraft's ability to survive fault conditions and autonomously recover from them, that the X2000 Program had a goal of developing non-volatile memory. The requirements of this memory were like no other: survive a high radiation environment (1 $MRad_{(Si)}$ TID), operate effectively and efficiently for a very long time (10 years), and sustain the ability to be addressed by the spacecraft computer twice every second for the purpose of storing spacecraft state and epoch: nearly a billion write cycles.

This paper will focus on the presentation of new technologies investigated and funded for development by JPL for this project. In addition to the challenge of an aggressive schedule, there are several main technical drivers which formed the impetus behind these developments: (i) non-volatility; (ii) an inordinately large number of write cycles without exhibiting fatigue; (iii) radiation tolerance to levels approaching 1 $MRad_{(Si)}$, (iv) density, (v) speed, and, (vi) power.

For X2000 the goal is to develop and characterize a standard series of spacecraft which could be readily re-configured to meet a mission's needs. For ease of testing and compatability, all of the avionic interfaces are based upon COTS technologies: Compact PCI (cPCI), $I^2C$, and IEEE-1394 (Firewire®) interfaces.

## AVAILABLE NVM

Since the advent of semiconductor memories in 1960s, when it replaced magnetic memories with its high density and superior performance, a tremendous advance has been made towards higher density, lower power consumption, extremely high speeds of memory access times, and lower costs. However, a truly nonvolatile memory that would retain its data without external power and can be programmed as a Static Random Access Memory (SRAM) or a dynamic RAM (DRAM), with a long life approaching 10 years, and suitable for NASA's mission requiring radiation tolerance in the Mega-Rad range is still not available [2].

A particular set of NASA requirements of radiation hardness combined with unlimited write cycles of $10^{13}$ during its 10-year life time provides a challenge that has defied solution so far.

Individually, these requirements have been satisfied using existing technologies; however, as a whole, they pose a challenge, which was so far unattainable. Several technologies, such as DRAM, exist wherein a large number of write cycles can be supported, but historically these devices are not tolerant of high total dose radiation; furthermore, these devices require substantial system-wide support in that they have a relatively high SEU rate in the cosmic environment, and lose data when powered off. Similarly, SRAM can be obtained with radiation tolerance, but, they, too, do not exhibit non-volatility.

Non-volatile memory devices exist today that are radiation tolerant such as Electrically Erasable Programmable Read Only Memory (EEPROM), but these devices have an inherent physical mechanism wherein fatigue is amplified during repeated write cycles – leading to the loss of ability to reliably store data. Eventual failure due to excessive writing is built in.

Current technology, as driven by the personal computer and commercial electronics markets, are focusing on the developments of various incarnations of Random Access Memories, and Flash memories. The former is approaching densities of 64 Mbits per die, but is volatile. The latter, being non-volatile, is rapidly gaining popularity. With sales expected to reach $3B in 1999, consumer demand for higher and higher density is emerging as the driver. Densities of 256 Mbits per die exist today [2]. However, this technology is presently faced with two apparently insurmountable limitations:

1. Endurance. Dependent on electron tunneling mechanisms, the device physics for the flash memories require that a high voltage be impressed on thin, fragile gate oxides to erase the device. Today's devices contain internal charge pump circuitry that increases the applied voltage, often 3.3 or 5 volts, to as high as 28 volts for the purposes of erasure, and 12 volts for the purposes of writing to a cell. Given a gate oxide 30 to 100Å thick, this voltage is extremely stressful to the device and will eventually lead to breakdown and ruination of a cell, if not the device.

2. Radiation. As mentioned earlier, the driver for the development of these devices is consumer demand. Recent testing by Jet Propulsion Laboratory and Goddard Space Flight Center teams of Samsung 128Mb and Toshiba 256Mb Flash memory parts indicates that the primary failure is the Charge Pump --- the very device that erases or writes to a device and cell [3]. Whereas earlier Flash devices (Intel 8 Mbit devices, for example) had connections for externally applied programming voltages, today's ultra-high density devices do not. In the bid for user simplicity the ability to survive in a radiation environment is lost.

## NEW MEMORY TECHNOLOGIES

The first customer of the X2000 Integrated First Delivery Project (IFDP) is also the one to traverse the worst radiation environment: NASA's Europa Orbiter (EO). EO is a mission to orbit the Jovian moon, Europa, and perform laser and radar sounding of the surface, The science objective of the EO mission is to determine the absence or presence of a subsurface ocean, characterize the 3-dimensional distribution of any subsurface and its overlying ice layers, understand the formation of surface features, sites of recent or current activity, and identify candidate landing sites for future missions. Observations from land and space-based instruments indicate that the surface of Europa is covered in water ice and thermal activity exists with sufficient energy as to allow the planet to remain bathed in liquid sea.

As Europa lies directly within the Jovian trapped ion belt, the radiation dose the planet is receiving is tremendous: calculations show that after one month in orbit, EO will have been exposed to over 4 Gigarads external to the spacecraft, and over 1 Megarad beneath the spacecraft's aluminum shell.

One requirement levied upon the X2000 Command and Data Handling subsystem is to permit rapid recovery upon a fault. With the mammoth Jovian gravitational influence, it may not have time to recover a wayward spacecraft before the mission would be lost. It is the intent of the CDH subsystem to write into protected, radiation tolerant memory the spacecraft time and status – perhaps as often as twice per second during critical operations. And to date, this type of memory: radiation tolerant, non-volatile, and capable of supporting nearly a billion write cycles, simply does not exist.

To take up this challenge, JPL has closely examined and selected three new technologies with a potential to bridge that technological gap to enable new missions to such places as Europa. However, a development-schedule to fulfill the technological as well as mission time requirements required many innovative solutions and untiring effort by the parts developers to not let the milestones slip.

In August 1998, via a Request for Information and follow-up personal visits, the Non-Volatile Memory industry was polled by JPL in order to ascertain the current state of the art and formulate plans for future development. It was determined that two technologies were of sufficient merit as to warrant JPL developmental funding:

1. Giant Magneto-Resistance Random Access Memory (GMRAM): Based on GMR effect, this technology is being developed by Honeywell's Solid State Electronics Center, Plymouth, Minnesota.
2. Ferro-Electric Random Access Memory (FERAM): Based on ferro-electric polarization effect, this technology is being developed by Celis Semiconductor, Colorado Springs, Colorado.

A third technology was also investigated during the first quarter of 1999 by JPL:

3. Chalcogenide memories. Based on material phase change (amorphous and polycrystalline) with temperature, this technology is being developed by Ovonyx, Troy, MI, and Mission Research Corporation, Albuquerque, NM.

A discussion of the current state of — and the JPL development effort for — these technologies is given below.

## GMRAM TECHNOLOGY

Honeywell's technology is based on Giant Magnetoresistance (GMR) effect reported by Baibich et al. in 1988 using magnetic superlattices grown by molecular beam epitaxy [4]. The GMR effect in superlattice is characterized by a 5-50% change in layer resistance when the magnetic field in the top layer is changed from parallel to anti-parallel with respect to the bottom layer. This change is a result of differences in spin-dependent scattering of electrons between the parallel and the anti-parallel states.

The GMRAM is a combination of GMR storage elements with a standard semiconductor underlayer on a silicon substrate. As shown in Figure 1, the GMR unit is a magnetic superlattice and consists of four thin layers separated in the middle by a thin copper layer. The five-layer sandwich from bottom to top thus consists of a thick NiFe storage layer, a CoFe GMR-enhancing layer, a Cu spacer layer, another CoFe layer, and finally, a thick NiFe reading layer. The deposition is done using an ultra high vacuum (UHV) ion beam deposition system. Advances in deposition technology have made it possible to deposit such uniform multilayer thin-films. The intersection of the bottom NiFe permalloy (sense line) and a metal layer (word line) defines the GMR memory bit. A digital metal line at the top is used for reversal of the magnetic field from a "0" to a "1" and vice versa, when required [5-7].

A major development program is already under way with DARPA-funded Spintronics effort [8] (along with funding from the Defense Threat Reduction Agency [DTRA]), which is helping to provide development funds to industry and academia including Honeywell's Solid State Electronics Center. Honeywell's scope under that effort is to develop and demonstrate commercial non-volatile 1Mb memory parts. Under this development effort, the focus is to develop and validate the commercial part prior to developing the radiation-hardened version. The JPL effort with Honeywell is intended to accelerate the development of the radiation-hardened version to meet the EO mission schedule.

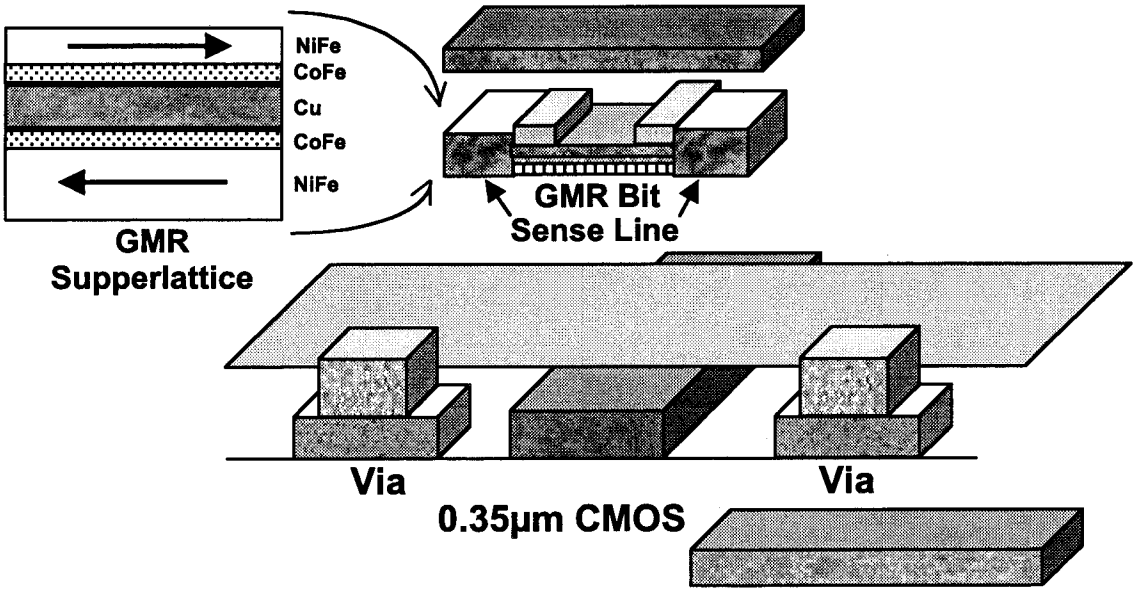


Figure 1. A GMR Overlayer sits over a CMOS Underlayer with metal lines forming the read-write connections. [Courtesy Honeywell]

This approach leverages and focuses the development towards production of parts with the specific mission requirements of radiation hardness and write cycles as described earlier. Initially, a short-term effort was initiated for Honeywell to study various technical issues about their technology that answered some of JPL's thermal, power, stability, and speed issues. Following this, a trade study was initiated to pinpoint all the design changes that would be needed to convert to a radiation-hardened version of the device including preliminary design of the 1 Megabit size package. During this phase, a parts-specification that would satisfy the NASA mission requirements was developed. A list of the same is provided in Table 1, which gives a comparative listing of the specifications for all three Non-Volatile technologies.

In addition, the trade study focused on the development of architecture and operation specifications. As a result of the trade study, power requirements was estimated to be 900 mW for write and 660mW for read operations. This power consumption being high was an issue that required close scrutiny. Architecture innovation caused it to be reduced by one half; even though it still remained on the high side. Honeywell is working on reducing the power further at the expense of slight increase in access times from 100-200ns to <300ns.

## FERROELECTRIC RAM TECHNOLOGY

The discovery of the ferroelectric effect dates back to 1921 in single crystal Rochelle salt and its extension to polycrystalline ceramics in 1940s with the realization of very high dielectric constant of barium tantalate capacitors. A history and technology of ferroelectric (FE) ceramics is given by Haertling [9]. Lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT) are especially of interest for nonvolatile memory and integrated circuit device applications. They possess very high dielectric constants (300 to 2000 based on constituents versus 3.9 for $SiO_2$, and 7.5 for $Si_3N_4$,), which makes very high-density devices possible with FE capacitors.

Ferroelectricity is the phenomenon of switching of the spontaneous polarization due to application of an electric field, and is present in such titanate compounds as barium, lead, and strontium. These materials are among several types designated as pyroelectric and possess, within a given temperature range, the unusual property of being permanently polarized. Further, the subgroup known as ferroelectrics consists of materials (SBT, PZT, etc.) whose dipole is changeable by application of an electric field (of magnitude less than the dielectric breakdown of the material).

When an electric field is applied, the $Ta^{5+}$ ion moves to a new position in a unit cell along the direction of the electric field, thereby polarizing the system in that direction. Reversing the electric field causes dipole reversal as "polarization-up" or "-down". When coherently present in a formulated bit, it would represent a "1" or a "0" for a memory bit. The polarization vs. electric field variation forms a typical hysteresis loop and is a very important characterization measurement. This is shown in Figure 2. Long-term stability of the polarized states have been established in SBT material and fabrication compatibility of SBT thin film deposition techniques with that of silicon devices has led to the development of high density memory devices.

Table 1. A comparative chart for memory specifications

| Feature | SRAM | DRAM | Flash | GMRAM | FERAM | C-RAM |
|---|---|---|---|---|---|---|
| **Non-Volatile** | No | No | Yes | Yes | Yes | Yes |
| **Operating Voltage, ± 10%** | 3.3 – 5 V | 3.3 V | 3.3 & 5 V | 3.3 V | 3.3 V | 3.3 V |
| **Organization (bits/die)** | 512K x 8 (rad hard) | 16M x 8 | 16M x 8, 32M x 8 | 128K x 8 | 16K x 8 | In Development |
| **Data Retention (@ 70° C)** | N/A | N/A | > 10 yrs | > 10 yrs | > 10yrs | > 10 yrs |
| **Endurance (Erase/Write Cycles)** | Unlimited | unlimited | $10^6$ (commercial) | $>10^{13}$ (design) | $>10^{13}$ (by test) | $10^{13}$ |
| **Access time, $t_{(acc)}$** | < 10 nS | <25 nS | 50 nS after page ready; 200µS Write; 2 mS erase | < 300 nS | < 300 nS | < 300 nS |
| **Radiation Total Dose Tolerance (Si)** | 1 MRad available | < 50 kRads | < 30 kRads | 1 MRad | 1 MRad | 1 MRad |
| **SEU rate (relative)** | Low to nil | High | nil (in cells); low to medium (device electronics) | nil | nil | nil |
| **Temp Range** | Mil-std. Available | Industrial | Commercial | Mil-std. | Mil-std. | Mil-std. |
| **Power** | 500 mW | 300 mW | 30 mW | 900 mW | 270 mW | In Development |
| **Package** | 4 Mb | 128 Mb | 128 Mb & 256 Mb | 1 Mb | 1.5 Mb (12 chip package) | In Development |

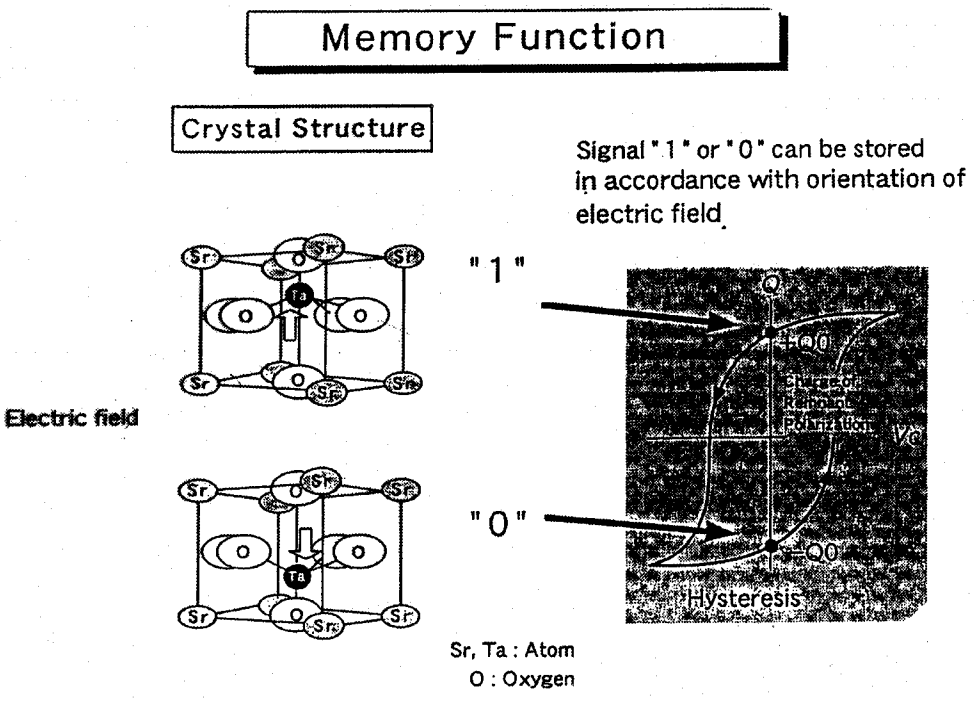


Figure 2. Inherent polarization (up & down) property of SBT material and a resulting hysteresis curve (Stored charge vs Electric Voltage) are shown. [courtesy Celis]

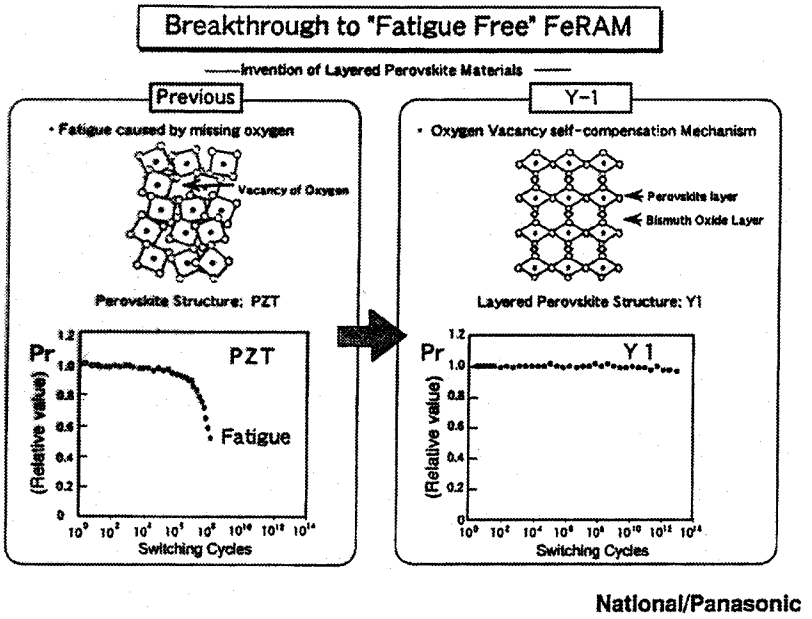


Figure 3. Layered Perovskite SBT shown on right has led to a fatigue free FERAM technology promise.

Figure 3 shows the structure of the layered material and the switching cycles ($>10^{13}$) without any visible degradation. [10-11]

Celis Semiconductor (a part of the Symetrix group of companies), an FE design house, was funded by JPL to perform this Non-Volatile RAM (NVRAM) development effort and given the overall responsibility to provide 1Mb radiation-hardened FE-based NVRAM packages required for X2000 1st Delivery. After a thorough search, they established that presently there were no U.S. companies with experience in fabricating radiation-hardened FE memories. Therefore, they established an international collaboration with Matsushita Electronics Corporation (MEC) who have extensive experience in volume manufacture (over one million RFID tags per month containing FE memory), and who were already involved with Celis for that effort.

As FE film is known to be inherently radiation hard, and because MEC did not have a radiation-hardened underlayer process (basic transistor structure), it was decided to build the underlayers at a U.S. foundry. Again, after a thorough search for a foundry with good process compatibility (MEC's 6" wafer processing foundry), the Sandia National Laboratories (SNL) was chosen as the partner for this effort. SNL would develop the underlayer processing to be compatible with the MEC processing technology of FE overlayer deposition. Therefore, an initial process development by SNL was successfully performed in consultation with MEC and Celis. Following this, a test chip was designed by Celis to be processed by SNL, followed by MEC processing to certify full compatibility.

During the beginning phase, Celis satisfied JPL concern on the issues of 10 year lifetime and $>10^{13}$ write cycles. In addition, the issue of hydrogen degradation was settled by subjecting memory bits in the RFID tag devices to high-dose alpha particles, which showed no degradation.

Originally Celis had decided to design their chips to contain 64Kb memory (8Kx8) per chip. Therefore, hand in hand with this effort, it was necessary for Celis to develop a preliminary package design for a part with a memory density of ~1Mb/in$^2$. Celis, in collaboration with Irvine Sensors Corporation, developed their CS2000XM multi-chip module (MCM) package concept. In order to maintain the package density, it was necessary to update their design and double their original chip density from 64Kb to 128Kb (16Kx8). This would double the number of memory cells per bit-line. However, it was determined that the bit-line capacitance would remain significantly the same because of the reduced junction capacitance obtained by the SNL-process. Thus, the bit-line signal to be sensed remained similar to that of the Celis memory design currently in volume production at MEC. In addition, it was realized that an alteration in the chip architecture and layout would keep the chip size from increasing.

For a 1Mb radiation-hardened package then, a 3-chip laminated design per layer and a four layer package with a total of twelve (12) 128Kb chips resulted in a 1"x1"

package with a total of 1.5Mb memory. The vertical package dimension restriction of 0.232" was also maintained as each layer could be designed with about 0.05" thickness [11-12].

This then paved the way for a first 128Kb (16Kx8) chip fabrication. The aggressive schedule required that the design of the 128Kb part be taken up concurrently with the fabrication and testing of the test chip. However, processing of wafers for the 128Kb part would be taken up only after the test chip would be fully tested and characterized. Since it was expected that the changes needed during the redesign phase would be minimal, a large part of the design time would have been usefully staggered. The projected chip parameters are given in Table 1.

## CHALCOGENIDE TECHNOLOGY

The semiconducting properties of a range of crystalline and amorphous chalcogenide alloys were investigated as early as the 1950s. In the early 1960s, new reversible phase-change materials and electrically and optically programmable devices were reported [13]. A number of recent developments, which include development for optical disk applications, more detailed understanding of the device behavior, and lithographic scaling and process improvement, have made it possible to use phase-change (and hence resistance change) semiconductor memory devices as practical high-performance memory elements [14].

The phase conversion (amorphous to polycrystalline and vice versa) is accomplished by heating and cooling the material. When heated to melting temperatures, it loses its crystalline structure and rapid cooling below glass transition temperature causes it to be locked into its amorphous (high resistance) phase. Near room temperature, this phase is very stable. However, the nucleation rate and crystallite growth increases exponentially as the temperature is raised near its melting point. To switch the memory element back to its polycrystalline (conductive) state, the material is heated to a temperature between the glass transition temperature and the melting temperature, causing nucleation and crystal growth to rapidly occur over a period of several nanoseconds.

The crystal nucleation and growth rate depend on the chalcogenide alloy composition and can vary by more than 20 orders of magnitude among various materials. Changes in the electrical properties of these alloys are far more dramatic, with variations in the electrical conductivity by up to 6 orders of magnitude between phases. The state of the cell, then, is determined by passing a regulated current through the cell and sensing the amount of voltage developed across it. Figure 4 shows the transition of phases and the conductivity and activation energy change with annealing temperature.

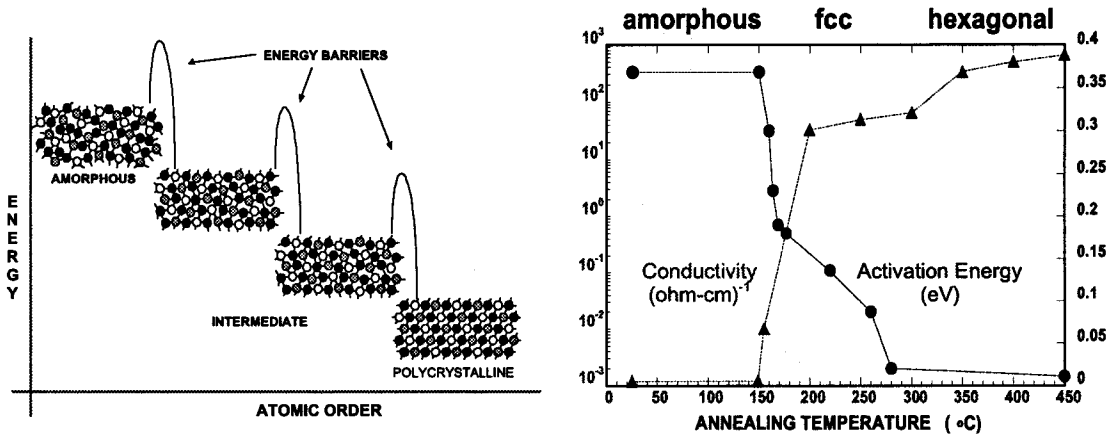


Figure 4. Chalcogenide phase change characteristics. [courtesy Ovonyx]

The nondestructive read/write is depicted by the resistance change uniformity over $10^{13}$ cycles operation shown in Figure 5.

To create an electronic memory from these materials, an array of access transistors must each be capable of providing sufficient power to a memory element to melt a portion of the chalcogenide alloy. Thermal isolation of the memory element itself from the heat-sinking substrate and metallization as well as neighboring cells (unintended phase change) is a crucial aspect of the memory element design.

Ovonyx and MRC have been pursuing the material and device research. Detailed modeling of the electrical, thermal and phase-transition behavior of these device

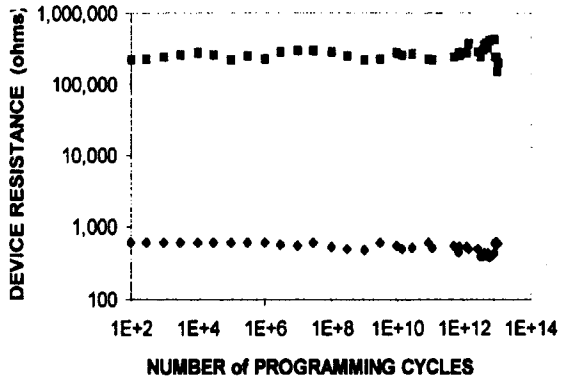


Figure 5. Resistance stability of the device with write cycles. [courtesy Ovonyx]

structures has been done. Alternative device structures to improve reliability are being looked into for integration into a standard CMOS logic or memory process. One structure currently being investigated by MRC is the bottom electrode contacting the chalcogenide alloy material and forming a ring-shaped contact area. The chalcogenide alloy is deposited in the highly conductive crystalline phase. The region where phase transition occurs is limited to the chalcogenide material immediately adjacent to the lower electrode. This reduction in the volume of material being melted reduces the power requirement sufficiently to allow a minimum-feature-size MOS transistor to easily control the device.

The Air Force Research Laboratory (AFRL) has funded an integration effort with the Mission Research Corporation (MRC) to demonstrate the feasibility of the technology. However, the schedule of their effort was found to be incompatible with the X2000 delivery requirement. Under the AFRL effort, the chalcogenide memory element will be integrated into the process flow of a radiation-hardened, submicron fabrication technology capable of supporting an initial circuit integration level of 16Mb [15].

## USE IN X2000

JPL also procuring a Non-Volatile Memory slice featuring a blend of non-volatile memory types: one is termed as Write Cycle Limited (WCL), and the other is termed as Unlimited Write Cycle (UWC). The UWC memory has been described in this paper, typically having an endurance level of $10^{13}$ cycles or more.

The memory card would utilize Flash memory technology for the WCL memory; and one of the two UWC memory depending upon a final selection based on maturity demonstration and an adherence to the schedule.

The card features a PCI interface with on-card control ASIC. The purpose of the ASIC is to provide data fetch and store operations, as well as Error Detection and Correction (EDAC) code generation and checking.

Two memory types (i.e. UWC and WCL) were specified as an interim because of the requirements and mission needs; however, a vendor was free to chose any singular technology, should it be shown suited to the tasks.

The following two tasks were specified for the mission:

1. Science data and computer boot images – this information would be kept in the WCL memory. For the most part, this memory is maintained in a benign state, being called upon only when necessary – typically at the end of the Cruise phase and immediately prior to and during the Science phase. Some missions have Cruise phases measured in years with the Science portion measured in weeks.
2. Spacecraft state, Machine state (CPU), and Spacecraft epoch (time) would be written frequently and would be retained in the memory in case of a sudden fault or power outage. This would utilize the services of the UWC memory. This memory would be written to at intervals ranging from sub-second to minutes depending upon mission status.

The following high-level requirements were specified for the memory card:

- Data capacity: 1-MByte Unlimited Write Cycle; 2-Gbit Write Cycle Limited, built-in EDAC
- Power 3.3 volt only, 2 watt maximum, during Write; 1 watt maximum during Read; 700 mW maximum during idle. Power control to the WCL memory.
- 3U Eurocard form factor; cPCI interface
- All parts certified to 1 $MRad_{(Si)}$, with the exception of the WCL memory, which is to be protected by a radiation shield clamshell as part of the card.

## CONCLUSIONS

Development effort and technological promises for radiation-hardened (1Mega-Rad total dose), unlimited-write ($>10^{13}$) cycles, non-volatile (>10 years) 1Mb memory suitable for future NASA missions is described.

Three different technologies, which were seriously considered (and two of them partly funded) are described in brief. A comparison chart for their individual promises is presented.

Looking at these new developments, it is believed that a new memory market of the 21st century will be established: that of the Radiation Hardened, Non-Volatile, Unlimited Write Cycle Memory, and that it will rapidly grow and expand in the course of just a few years. This development alone will usher in a change in the way things are done enabling exciting new applications.

## ACKNOWLEDGMENTS

The review described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a Contract with the National Aeronautics and Space Administration.

Reference herein to any specific commercial product, process or service by trade name, trade mark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

We express our deep appreciation for GMRAM data and graphics received from and in-depth discussions with Mr. H. Kaakani, Dr. R.R. Katti and the Honeywell GMRAM development team. Similarly, we wish to thank Mr. S.C. Philpy and the Celis Development Team for detailed discussions, and sharing of data and graphics for the FERAM. In addition, we express our gratitude to Mr. Scott Tyson for sending the graphics and data for their CRAM technology and suggestions for the paper. Further, the authors would like to thank Dr. L. Alkalai, and Mr. E. Holmberg for their suggestions and useful discussions.

## REFERENCES

[1.] Presentations at the NASA/JPL International Conference on Electronics for Extreme Environments, Feb. 1999, Pasadena, CA.

[2.] *"Nonvolatile Semiconductor Memory Technology,"* Ed: W.D. Brown and J.E. Brewer, IEEE Press, New York, 1998.

[3.] D.N. Nguyen, S. Guertin, G.M. Swift, J. Coss, and A.H. Johnston, "radiation Effects on Advanced Flash Memories," Proc. Of the 1999 IEEE Nuclear and Space Radiation Effects Conference, Norfolk, Virginia, July, 1999.

[4.] M.N. Baibich, J.M. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Eitenne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant Magnetoresistance of (001)Fe/(001) Cr Magnetic Superlattices," Physical Review Letters, vol. 61, 24722475, 1988.

[5.] R. Katti and H. Kaakani. "GMRAM: Giant Magneto-Resistance Random Access Memory," Proc. of the 2000 IEEE Aerospace Conference, Big Sky, Montana, March 18-25, 2000.

[6.] J. Gadbois, J.-G. Zhu, W. Vavra, and A. Hurst. "The Effect of End and Edge Shape on the Performance of Pseudo-Spin Valve Memories," IEEE Transactions on Magnetics, Vol. 34, No. 4, July, 1998, pp. 1066-1068.

[7.] J. Shi, T. Zhu, M. Durlam, E. Chen, S. Tehrani, Y. Zheng, and J. Zhu. "End Domain States and Magnetization Reversal in Submicron Magnetic Structures," IEEE Transactions on Magnetics, Vol. 34, No. 4, July, 1998, pp. 997-999.

[8.] Record of the Abstracts for DARPA's Third Annual Sprintronics Workshop and Review, White Plains, New York, July 8-10, 1999.

[9.] G.H. Haertling, "Ferroelectric Ceramics: History and Technology," Journal of the American Ceramic Society, Vol. 82, 797-818, 1999.

[10.] O. Auciello, J. Scott, and R. Ramesh, "The Physics of Ferroelectric Memories," *Physics Today*, American Institute of Physics, July 1998, pp. 22-27.

[11.] S.C. Philpy, D.A. Kamp, T.A. Meester, A.D. DeVilbiss, A.F. Isaacson, and G.F. Derbenwick, "Reliability of Ferroelectric Memory for High-Rel and Space Applications," JPL/2nd Annual Microelectronics Reliability and Qualification Workshop, Pasadena, CA; Oct. 26-27, 1999; Session VIII.

[12.] S.C. Philpy, D.A. Kamp, A.D. DeVilbiss, A.F. Isaacson, and G.F. Derbenwick, "Ferroelectric Memory Technology for Aerospace Applications," Proc. 2000 IEEE Aerospace Conference, Big Sky, Montana, March 18-25, 2000.

[13.] S. Ovshinsky, "Reversible Electrical Switching Phenomena in Disordered Structures," Phys. Rev. Lett., v21, no20, pp1450-1453, November 11, 1968.

[14.] S. Ovshinsky, "Amorphous Materials- The Key to New Devices," IEEE Proc. of CAS, vol. 1, pp. 33, 1998.

[15.] S. Tyson, T. Lowrey, S. Hudgens, G. Wicker, and K. Hunt, "Nonvolatile, High Density, High Performance Phase-Change Memory," Proc. 2000 IEEE Aerospace Conference, Big Sky, Montana, March 18-25, 2000.

**Karl F. Strauss** is a Senior Engineer at JPL, and has been in their employ for 14 years. Karl has 25 years of aerospace industry design experience, most of it concentrated on various memory types: everything from Core to Tape to Solid State. His work can be found on many of today's commercial and military aircraft, as well as missions to Venus, Mars, Saturn, and Jupiter. Before joining the X2000 team, Karl led the development of the Solid State Recorder for the Saturn-bound Cassini mission. He is named on a patent regarding memory storage technology.

**Taher Daud**, a device physicist, is a member of the technical staff at JPL for the past 23 years. He has worked on a variety of electronic device technologies including solar cells, charge-coupled devices, neural networks, fuzzy logic, expert system and evolvable hardware. Currently, he is also involved with nonvolatile memory development for X2000 project. He has published/presented over 70 papers and is named on several patents.